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Karen Vertz

(Depositor's name)

Karen Vertz
5-26-05

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,575	09/16/2003	Vikas K. Agrawal	TI-35282	2989

TITLE OF INVENTION: CYCLE READY CIRCUIT FOR SELF-CLOCKING MEMORY DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$300	\$1700	08/16/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, VAN THU T	2824	365-233000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
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2. For printing on the patent front page, list
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1 **Alan K. Stewart**
2 **W. James Brady, III**
3 **Frederick J. Telecky, Jr.**

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
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Texas Instruments Incorporated(B) RESIDENCE: (CITY and STATE OR COUNTRY)
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☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

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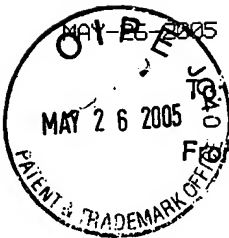
Alan K. StewartDate **5/26/05**Registration No. **35,373**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Applicant **Vikas K. Agrawal**

Docket Number: **TI-35282**

Serial No.: **10/663,575**

Art Unit: 2824

Filed: 09/16/03

Examiner: Van Thu T. Nguyen

For: **Cycle Ready Circuit for Self-Clocking Memory Device**

CERTIFICATION OF FACSIMILE TRANSMISSION	
I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below:	
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NAME OF INVENTOR(S): Prasun K. Raha		RECEIPT DATE & SERIAL NO.: Serial No.: 10/663,575
TITLE OF INVENTION: Cycle Ready Circuit for Self-Clocking Memory Device		Filing Date: 09/16/03
TI FILE NO.: TI-35282	DEPOSIT ACCT. NO.: 20-0668	
FAXED: 5-26-05 DUE: 8-16-05 ATTY/SECY: AKS/kjv		

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